THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte DAVID E. BOERSTLER, EDWARD B. EICHELBERGER, GARY T. HENDRICKSON and CHARLES B. WINN

Appeal No. 95-4531
Application No. 07/939,892[1]

ON BRIEF

Before HAIRSTON, KRASS, and BARRETT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 26. In an Amendment[2] After Final (paper number 13), claims 5, 17, 21, 22, and 26 were amended.

The disclosed invention relates to a level shift circuit for a logic circuit that translates a first voltage level binary

[1] Application for patent filed September 1, 1992.

[2] As indicated in the Advisory Action (paper number 14), the amendment had the effect of overcoming the indefiniteness rejection of claims 17 through 21.

pulse signal at an input node to a second voltage level at an output node coupled to a capacitive load.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A level shift circuit for a logic circuit for translating a first voltage level binary pulse signal from said first voltage level at an input node to a second voltage level at an output node coupled to a capacitive load, said circuit comprising:

a resistor connected to a DC supply voltage;

diode means with a capacitance substantially higher than that of the capacitive load for creating the voltage level translation connected in series with said resistor and having a first and a second terminal, wherein said second terminal forms said output node at the point of interconnection of said resistor and said diode means;

said first voltage level binary pulse signal connected to said diode means at said first terminal which is said input node, and said second voltage level pulse signal appearing at said output node.

The references relied on by the examiner are:

Davis	3,535,546	Oct. 20, 1970
Eden (U.K. patent application)	2,166,312	Apr. 30, 1986

Sedra et al. (Sedra), “Microelectronic Circuits,” Holt, Rinehart and Winston, Inc., pages 170, 171, 195 and 453, 1987.

Claims 1, 2, 4 through 9, 14 through 24 and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sedra in view of Eden.

Claims 3, 10 through 13 and 25 stand rejected under

35 U.S.C. § 103 as being unpatentable over Sedra in view of Eden and Davis.

Reference is made to the brief[3] and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1 through 26.

Sedra discloses a resistor and a diode in series between a positive voltage and ground (Figures 4.15 and P4.1). According to the examiner (Answer, page 3):

> Eden shows a "capacitance substantially higher than that of the capacitive load" in Figure 1, element 10 (see also page 2, lines 52-57). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have added the capacitor 10 in parallel with Sedra et al.'s diode for the purpose of increasing switching speed as taught by Eden on page 2, lines 55-58.

Appellants argue (Brief, pages 5 and 6) that the circuits in Figures 4.15 and P4.1 of Sedra do not perform any switching functions because both figures show a diode and a resistor

[3] Neither of the reply briefs (paper numbers 22 and 24) was entered by the examiner. Appellants' Petition to the Commissioner (paper number 26) was dismissed (paper number 27).

connected in series between a fixed voltage and ground.

Appellants also argue (Brief, page 7) that:

> Secondly, the diode means in the proposed combinations can't be connected between the input and output nodes of the circuit with a "first level binary pulse signal connected to the diode means at said input node" and having a "second voltage level pulse signal appearing at said output node" as claimed in paragraph 4 of claim 1. As pointed out previously, one terminal of the two terminal diode means of both proposed combinations is connected to a fixed potential. With one of two terminals fixed, it is impossible to provide a binary input pulse at one of the terminals and obtain a binary output pulse on the other of the two terminals.

We agree with appellants. The obviousness rejection of claims 1, 2, 4, 5, 8, 9, 16 through 24 and 26 is reversed.

The examiner recognizes (Answer, page 4) that Sedra's emitter follower circuit (Figure 8.41) has collector and emitter terminals "connected directly opposite to the collector and emitter terminals" in claim 6, but nevertheless concludes that "[i]t would have been obvious to one of ordinary skill in the art, at the time of the invention, to have switched the connections of Sedra et al.'s transistors for the purpose of utilizing the inherent larger collector-base capacitance of Sedra et al.'s circuit as described by Eden on page 2, lines 52-55."

Appellants argue (Brief, page 8) that:

> The emitter follower of Figure 8.41 does not show as claimed in claim 6: a) "an emitter connected to a

> common potential"; b) "a capacitance load....connected to the collector node"; or c) "the transistor being biased so that the emitter-base junction of said transistor is reversed biased".
>
> To make Figure 8.41 read on this language in claim 6, it would require a complete reorganization of the circuit elements of the circuit of Figure 8.41 so that it would not [sic, no] longer perform its emitter follower function. There is no teaching in Eden to do this.

We agree with appellants. The obviousness rejection of claims 6 and 14 is reversed.

Turning next to claims 7 and 15, the examiner contends (Answer, pages 4 and 5) that "[i]t would have been obvious to one of ordinary skill in the art, at the time of the invention, to have substituted Sedra et al.'s single diode with a 'bipolar transistor ... with its collector and emitter shorted' as such a substitution provides more current to the load and hence a faster switching speed." Appellants argue (Brief, page 10) that the claimed bipolar transistor forward biased at its collector-base junction, and shorted at its collector and emitter would not have

been rendered obvious by the single diode teachings of Sedra. We agree with appellants. The obviousness rejection of claims 7 and 15 is reversed.

Turning lastly to claims 3, 10 through 13 and 25, the examiner cited Davis for "a 'diode-connected transistor' (36) in Figure 1." (Answer, page 5 and 6). We agree with appellants' argument (Brief, page 14) that Davis does not make up "for the failings of the Sedra circuits of Figures P4.1 and 4.15." The obviousness rejection of claims 3, 10 through 13 and 25 is reversed.

DECISION

The decision of the examiner rejecting claims 1 through 26 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
ERROL A. KRASS Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LEE E. BARRETT Administrative Patent Judge	)

Appeal No. 95-4531
Application No. 07/939,892

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Appeal No. 95-4531
Serial No. 07/939,892

Judge HAIRSTON

Judge KRASS

Judge BARRETT

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DECISION: REVERSED

Send Reference(s): Yes No
or Translation(s)

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Index Sheet-2901 Rejection(s): _____

Acts 2: ____

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